REMARKS

Applicants respectfully request reconsideration of the present U.S. patent application. Claims 1, 2 and 4-22 stand rejected under 35 U.S.C. § 103. Claims 1 and 2 have been amended. Claim 23 has been added. No claims have been canceled. Therefore, Claims 1, 2 and 4-23 are pending.

Claim Rejections - 35 U.S.C. § 103

Rejections of Claims 1, 4, 6-11, 13, 14, 16-18, 20 and 21 based on *Otani* and *Holt*

Claims 1, 4, 6-11, 13, 14, 16, 17, 18, 20 and 21 have been rejected by Examiner under 35 U.S.C. §103 as being unpatentable over U.S. Patent Application 2001/0022534 filed by Otani (*Otani*), in view of electronic Circuits – Digital and Analog by Holt (*Holt*). For at least the reasons set forth below, Applicants submit that Claims 1, 4, 6-11, 13, 14, 16-18, 20 and 21 are not rendered obvious by *Otani* in view of *Holt*.

Claim 1 recites the following:

> an impedance inverter circuit configured to provide impedance inversion and introduce a first path delay to the first path output signal, thereby creating a first path delayed output signal; ...
>
> and
>
> a bias control circuit configured to provide a first bias voltage that enables the first subsection of the first amplifier and the first subsection of the second amplifier, to cause the enabled subsections to operate in a linear mode during a low power mode, wherein the second subsection of the first amplifier and the second subsection of the second amplifier are disabled in the low power mode, and a second bias voltage that enables the second subsection of the first amplifier and the second subsection of the second amplifier, , wherein the first subsection of the first amplifier and the first subsection of the second amplifier are enabled in the high power mode, to cause the enabled amplifier subsections to operate in a linear mode during a high power mode.

Claims 13 and 23 recite similar limitations.

Examiner contends that *Otani* discloses all the elements of Claim 1 and 13 except a bias circuit to an amplifier. *Otani* discloses a power amplifier that comprises phase

converters. See Fig. 2; paragraph [0029]. The phase converters contain a distributing circuit to split or combine signals and a phase adjusting circuit to synthesize antiphase signals. See Fig. 1; paragraph [0022].

According to the Examiner, capacitor C8, inductor L7 and capacitor C10 of *Otani* constitute an impedance inverter circuit. However, *Otani*'s distributing circuit contains two capacitor-inductor-capacitor components, which serve as signal combiners. This arrangement has the net effect of providing no impedance inversion. Therefore, *Otani* does not disclose an impedance inverter circuit. Consequently, *Otani* fails to disclose at least one limitation of claims 1, 13 and 23.

Examiner cites *Holt* for the proposition that the use of a bias control circuit would have been obvious because "it is well known to provide a bias circuit to an amplifier." See Office Action page 3. *Holt* does not disclose an impedance inverter circuit, and therefore fails to cure the deficiencies of *Otani* pointed out by Applicants. In addition, although Applicants agree with Examiner that a bias control circuit is a necessary part of an amplifier circuit, *Holt* teaches no more than basic principles and theories of electronic circuits. *Holt* does not disclose the bias control circuit recited in claims 1, 13 and 23.

Neither *Otani* nor *Holt* teaches or suggests a power amplifier comprising the impedance inverter circuit or the bias control circuit recited in claims 1, 13 and 23. Thus, *Otani* in view of *Holt* fails to disclose at least one limitation of claims 1, 13 and 23. Consequently, claims 1, 13 and 23 are not rendered obvious by *Otani* in view of *Holt* for at least the reasons set forth above. Applicants therefore respectfully request that the Examiner withdraw the rejections of claims 1 and 13 under 35 U.S.C. § 103.

Claims 4 and 6-11 depend from Claim 1. Claims 14, 16-18, 20 and 21 depend from Claim 13. Because dependent claims include the limitations of the claims from

which they depend, Applicants submit that Claims 4, 6-11, 14, 16-18, 20 and 21 are not rendered obvious by *Otani* in view of *Holt* for at least the reasons set forth above.

Rejections of Claims 2 and 15 based on *Otani*, *Holt* and *Cheng*

Claims 2 and 15 have been rejected under 35 U.S.C. § 103 as being unpatentable over *Otani* in view of *Holt*, and further in view of *Cheng* et al., U.S. Patent Application No. 2002/0190790 (*Cheng*). For at least the reasons set forth below, Applicants submit that Claims 2 and 15 are not rendered obvious by *Otani* in view of *Holt* and *Cheng*.

As explained above, *Otani* in view of *Holt* fails to disclose a power amplifier comprising the impedance inverter circuit or bias control circuit recited in claims 1 and 13. Examiner cites *Cheng* as teaching selectively supplying bias voltages to parallel-connected amplifiers. See Office Action, page 5.

Applicants do not necessarily agree with the Examiner's characterization of *Cheng*, and expressly reserve the right to address the Examiner's characterization of *Cheng* in any future Office Actions. However, regardless of whether Examiner's characterization of *Cheng* is correct, *Cheng* fails to cure the deficiencies of *Otani* in view of *Holt* pointed out by Applicants. Consequently, claims 1 and 13 are not rendered obvious by *Otani* in view of *Holt* and *Cheng* for at least the reasons set forth above.

Claim 2 depends from claim 1. Claim 15 depends from claim 13. Because dependent claims include the limitations of the claims from which they depend, Applicants submit that claims 2 and 15 are not rendered obvious by *Otani* in view of *Holt* and *Cheng* for at least the reasons set forth above. Applicants therefore request that the Examiner withdraw the rejections of claims 2 and 15 under 35 U.S.C. § 103.

Rejections of Claims 5 and 19 based on *Otani*, *Holt* and *Sedra*

Claims 5 and 19 were rejected under 35 U.S.C. § 103 as being unpatentable over *Otani* in view of *Holt*, and further in view of *Sedra*. For at least the reasons set forth below, Applicants submit that Claims 5 and 19 are not rendered obvious by *Otani* in view of *Holt* and *Sedra*.

As explained above, *Otani* in view of *Holt* fails to disclose a power amplifier comprising the impedance inverter circuit or bias control circuit recited in claims 1 and 13. Examiner cites *Sedra* with regard to replacing single-stage amplifiers with multiple-stage amplifiers. See Office Action, pages 5-6.

Applicants do not necessarily agree with the Examiner's characterization of *Sedra*, and expressly reserve the right to address the Examiner's characterization of *Sedra* in any future Office Actions. However, regardless of whether the Examiner's characterization of *Sedra* is correct, *Sedra* fails to cure the deficiencies of *Otani* in view of *Holt* pointed out by Applicants. Thus, *Otani* in view of *Holt* and *Sedra* fails to disclose at least one limitation of claims 1 and 13. Consequently, claims 1 and 13 are not rendered obvious by *Otani* in view of *Holt* and *Sedra* for at least the reasons set forth above.

Claim 5 depends from claim 1. Claim 19 depends from claim 13. Because dependent claims include the limitations of the claims from which they depend, Applicants submit that claims 5 and 19 are not rendered obvious by *Otani* in view of *Holt* and *Sedra* for at least the reasons set forth above. Applicants therefore request that the Examiner withdraw the rejections of claims 5 and 19 under 35 U.S.C. § 103.

Rejections of Claims 12 and 22 based on *Otani*, *Holt* and *Taniguchi*

Claims 12 and 22 were rejected under 35 U.S.C. § 103 as being unpatentable over *Otani* in view of *Holt*, and further in view of U.S. Patent No. 5,162,756 issued to Taniguchi et al. (*Taniguchi*). For at least the reasons set forth below, Applicants submit that Claims 12 and 22 are not rendered obvious by *Otani* in view of *Holt* and *Taniguchi*.

Examiner does not assert that *Sedra* discloses or suggests a skilled artisan employ an impedance inverter circuit in conjunction with a bias change as power modes Examiner cites *Taniguchi* with regard to replacing single-stage amplifiers with multiple-amplifier arrangements. See Office Action, pages 6-7.

Applicants do not necessarily agree with the Examiner's characterization of *Taniguchi*, and expressly reserve the right to address the Examiner's characterization of *Taniguchi* in any future Office Actions. However, regardless of whether Examiner's characterization of *Tanaguchi* is correct, *Taniguchi* fails to cure the deficiencies of *Otani* in view of *Holt* pointed out by Applicants. Thus, *Otani* in view of *Holt* and *Taniguchi* fails to disclose at least one limitation of claims 1 and 13. Consequently, claims 1 and 13 are not rendered obvious by *Otani* in view of *Holt* and *Taniguchi* for at least the reasons set forth above.

Claim 12 depends from claim 1. Claim 22 depends from claim 13. Because dependent claims include the limitations of the claims from which they depend, Applicants submit that claims 12 and 22 are not rendered obvious by *Otani* in view of *Holt* and *Taniguchi* for at least the reasons set forth above. Applicants therefore request that the Examiner withdraw the rejections of claims 12 and 22 under 35 U.S.C. § 103.

CONCLUSION

For at least the foregoing reasons, Applicants submit that the rejections have been overcome. Therefore, claims 1, 2 and 4-23 are in condition for allowance and such action is respectfully solicited. The Examiner is respectfully requested to contact the undersigned by telephone if such contact would further the examination of the present application.

Respectfully submitted,

Dated: May 16, 2007

Joseph A. Pugh
Reg. No. 52,137
TriQuint Semiconductor, Inc.
2300 NE Brookwood Parkway
Hillsboro, OR 97124
(503) 615-9616